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Park et al.(10) **Pub. No.: US 2016/0247870 A1**(43) **Pub. Date: Aug. 25, 2016**(54) **ORGANIC LIGHT-EMITTING DIODE
DISPLAY AND METHOD OF
MANUFACTURING THE SAME**(71) Applicant: **Samsung Display Co., Ltd.,**
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Seongkweon Heo, Yongin-City (KR)(21) Appl. No.: **14/806,013**(22) Filed: **Jul. 22, 2015**(30) **Foreign Application Priority Data**

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27/1288 (2013.01); **H01L 2227/323** (2013.01)(57) **ABSTRACT**

An organic light-emitting diode (OLED) display and a method of manufacturing an OLED display are disclosed. In one aspect, the display includes a substrate and a thin-film transistor including an active layer, a gate electrode, a source electrode, and a drain electrode formed over the substrate. A gate insulating layer is formed between the active layer and the gate electrode, and an interlayer insulating layer is formed between the gate electrode and the source and drain electrodes. Also, a planarization layer is formed over the source and drain electrodes, and a pixel electrode is formed over the planarization layer. The display also includes capacitor including a first electrode formed on the same layer as the active layer and a second electrode formed of the same material as the pixel electrode. A pixel-defining layer covers opposing ends of the pixel electrode; an emission layer formed over the pixel electrode.

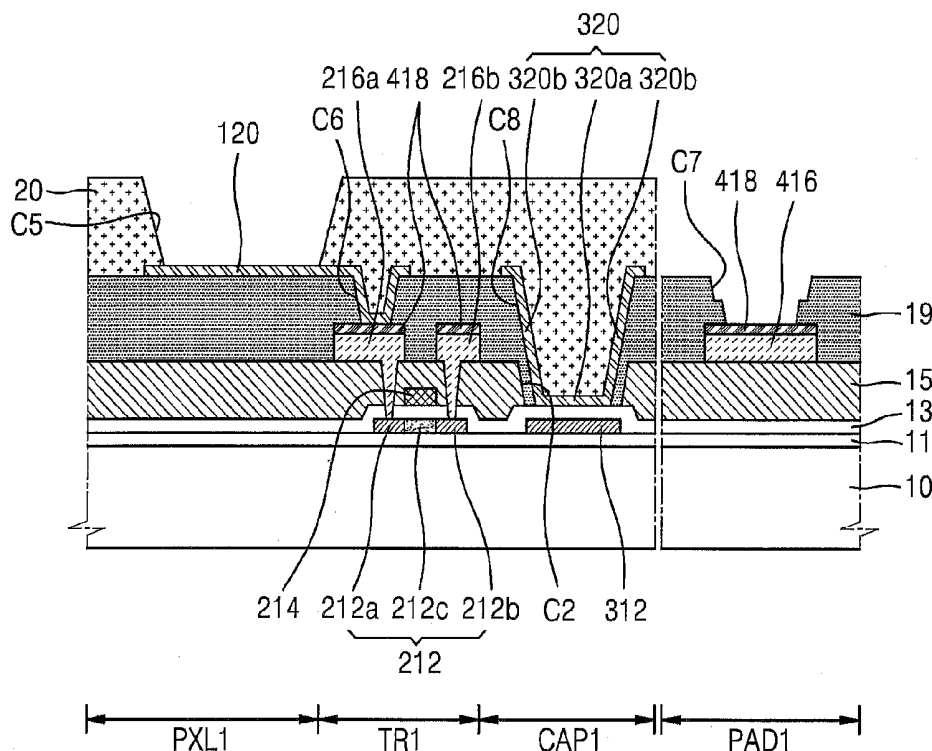
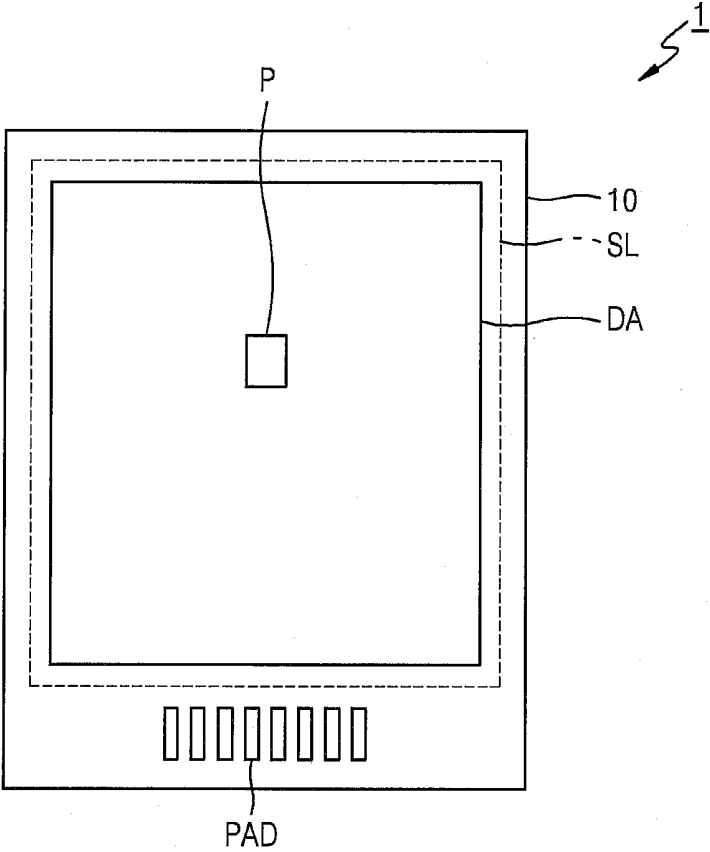


FIG. 1



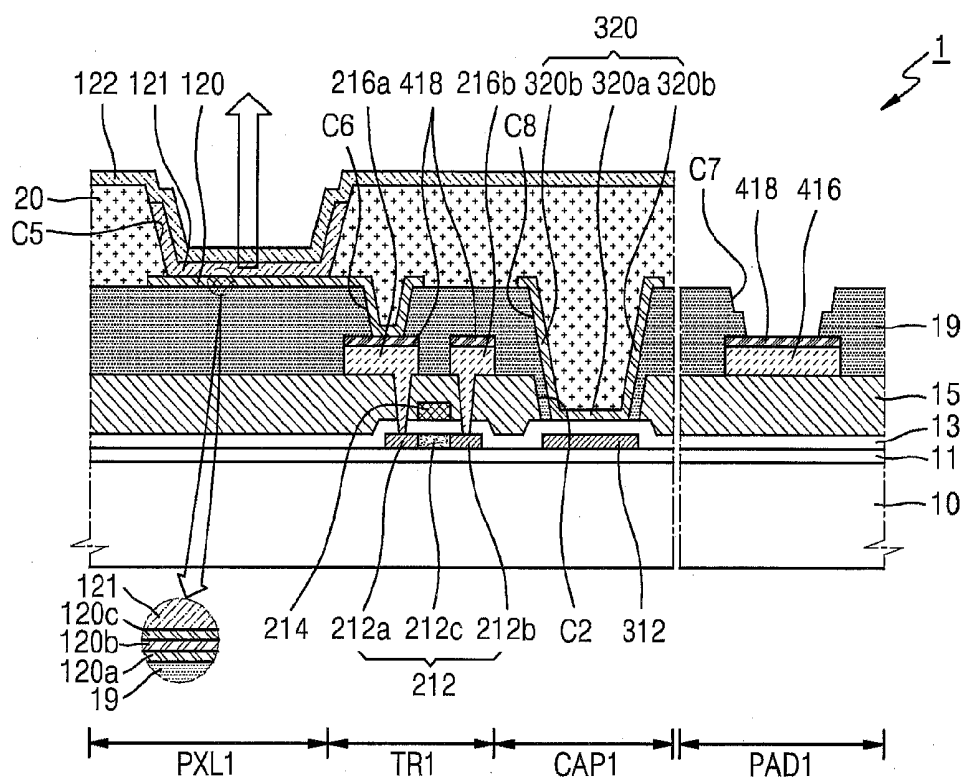


FIG. 3

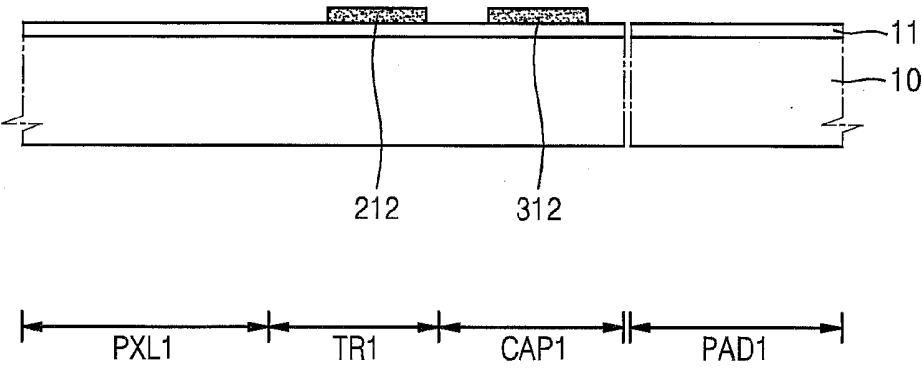


FIG. 4A

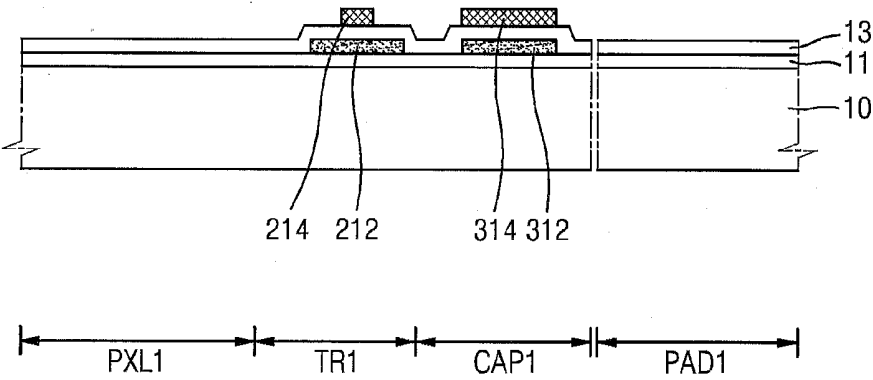


FIG. 4B

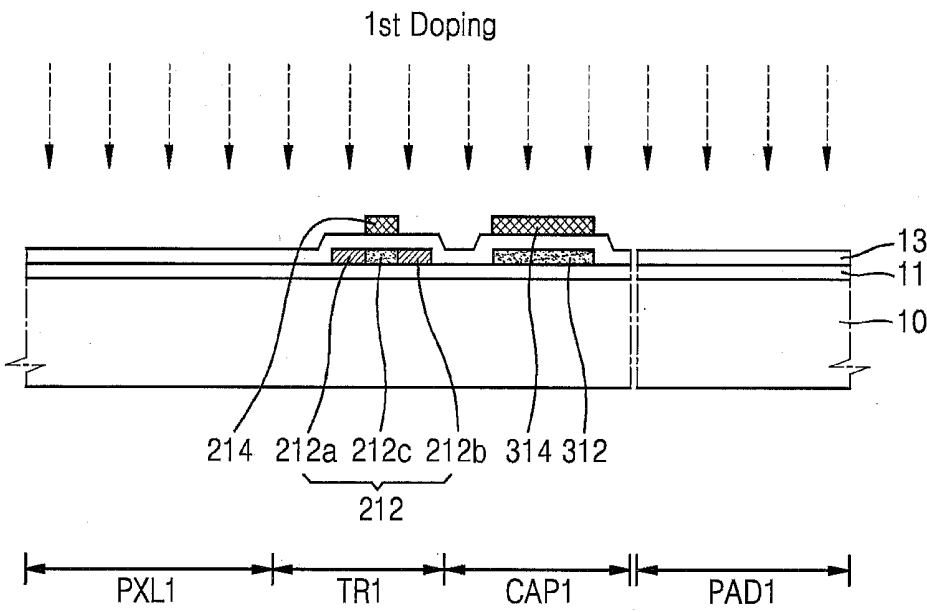


FIG. 5

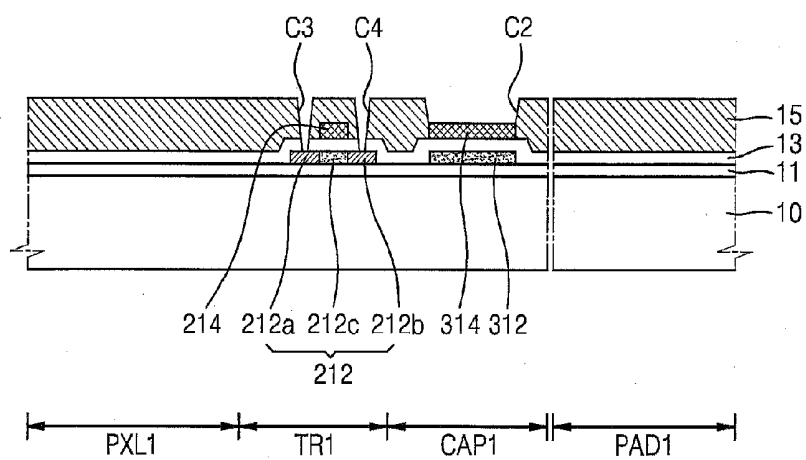
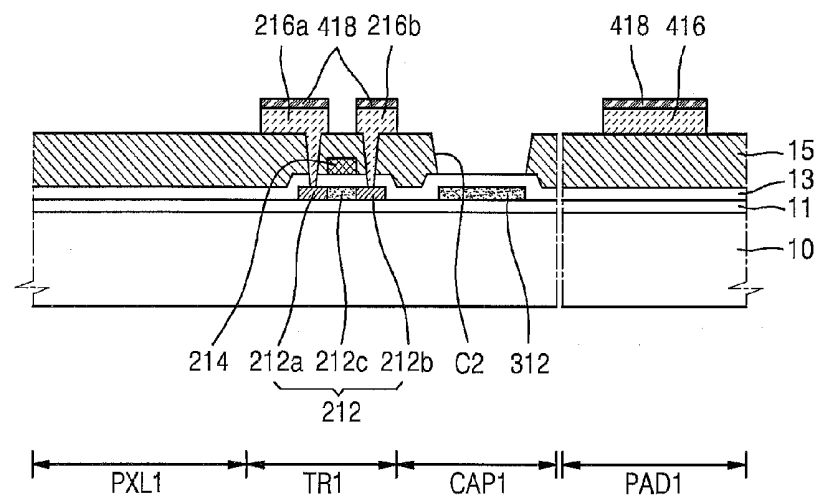


FIG. 6A



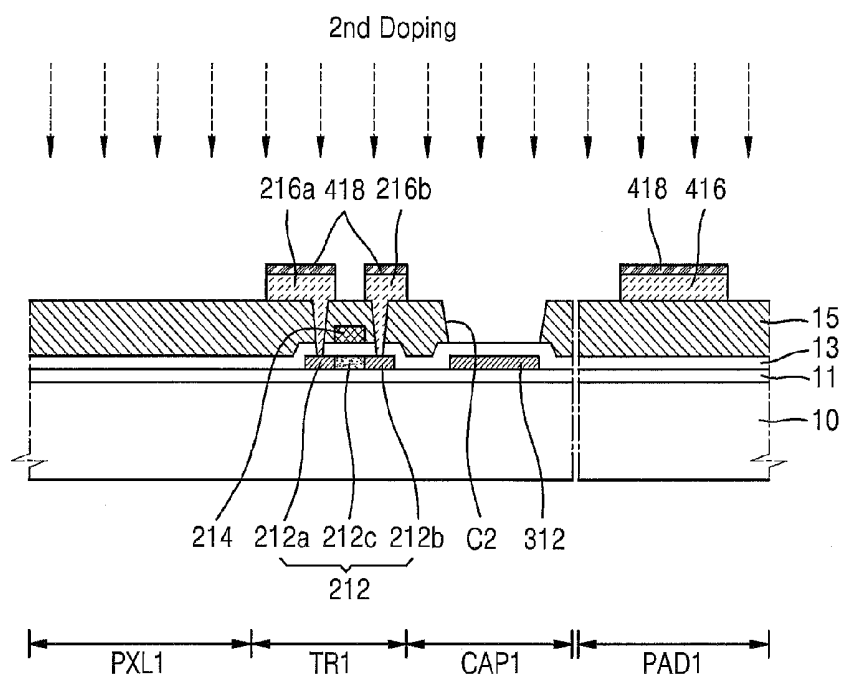


FIG. 7

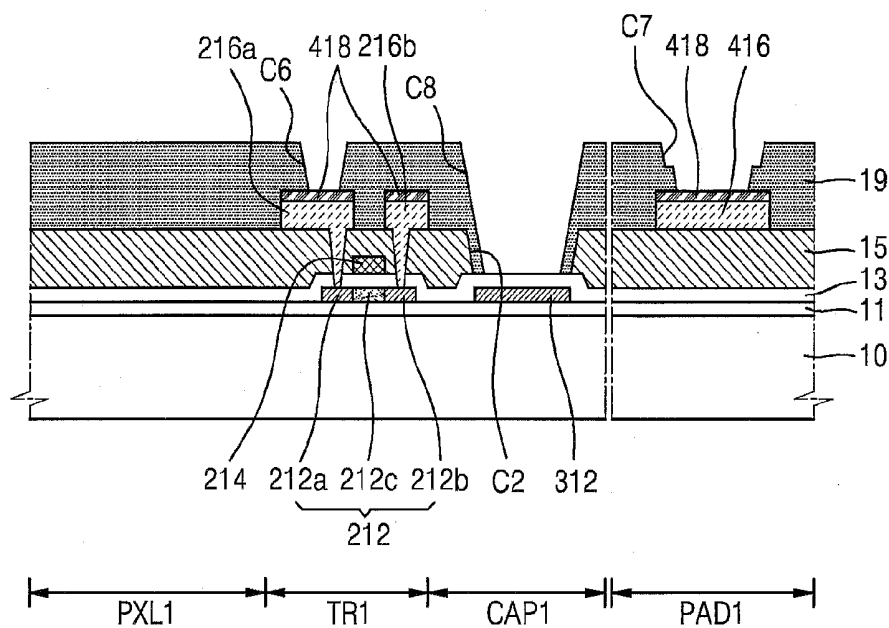


FIG. 8

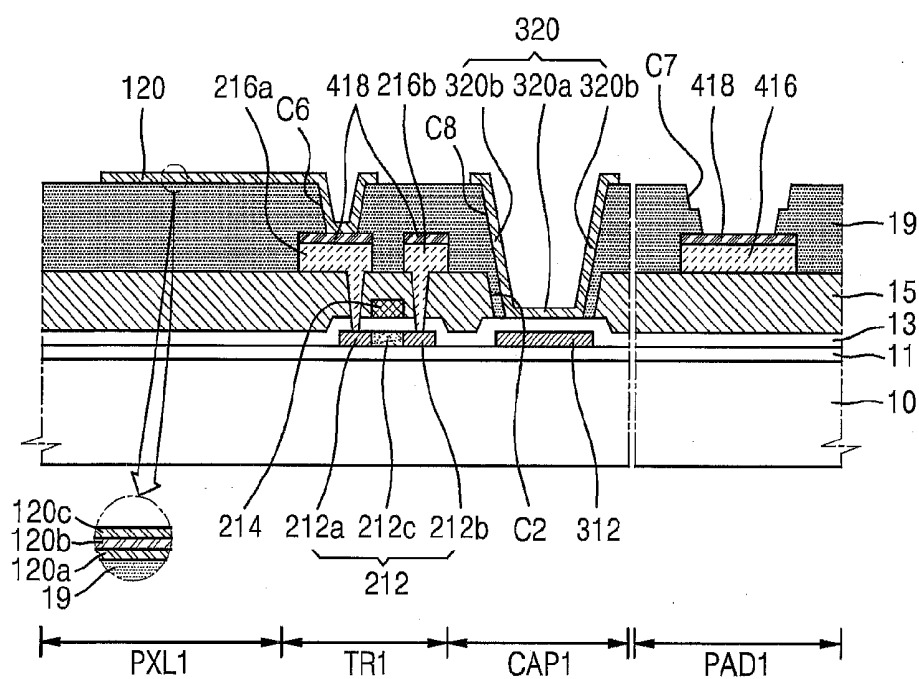
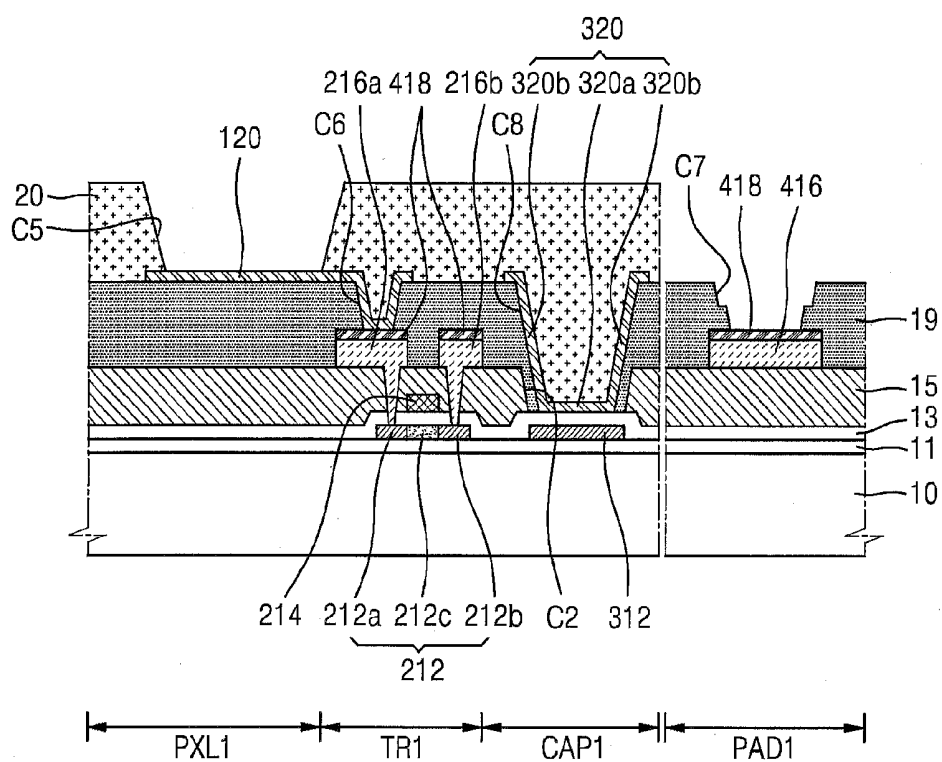


FIG. 9



ORGANIC LIGHT-EMITTING DIODE DISPLAY AND METHOD OF MANUFACTURING THE SAME

RELATED APPLICATION

[0001] This application claims the benefit of Korean Patent Application No. 10-2015-0025917, filed on Feb. 24, 2015, in the Korean Intellectual Property Office, the disclosure of which is incorporated herein in its entirety by reference.

BACKGROUND

[0002] 1. Field

[0003] The described technology generally relates to an organic light-emitting diode display and a method of manufacturing the same.

[0004] 2. Description of the Related Art

[0005] An organic light-emitting diode (OLED) display is a self-emissive display that generally includes a hole injection electrode, an electron injection electrode, and an emission layer formed therebetween. During operation, holes injected from the hole injection electrode and electrons injected from the electron injection electrode are re-combined in the emission layer so that light is emitted therefrom. The OLED display is anticipated as a next generation display due to its favorable characteristics such as low power consumption, high contrast, fast response speed, etc.

SUMMARY OF CERTAIN INVENTIVE ASPECTS

[0006] One inventive aspect relates to an OLED display and a method of manufacturing the same.

[0007] Another aspect is an OLED display that includes a substrate; a thin-film transistor including an active layer, a gate electrode, a source electrode, and a drain electrode formed on the substrate; a gate insulating layer formed between the active layer and the gate electrode; an interlayer insulating layer formed between the gate electrode and the source and drain electrodes; a planarization layer formed on the source electrode and the drain electrode; a pixel electrode formed on the planarization layer; a capacitor including a first electrode formed from a same layer as the active layer and a second electrode formed of a same material as the pixel electrode; a pixel-defining layer covering edges of the pixel electrode; an emission layer formed on the pixel electrode; and an opposite electrode formed on the emission layer.

[0008] The first electrode can include an ion impurity-doped semiconductor.

[0009] A bottom surface of the second electrode can directly contact the gate insulating layer.

[0010] The interlayer insulating layer can include a first opening formed in the first electrode, the planarization layer can include a second opening formed in the first opening and having a width less than a width of the first opening, and the second electrode can be formed in the second opening.

[0011] The planarization layer can cover side surfaces of the first opening formed in the interlayer insulating layer.

[0012] A top surface of the second electrode can directly contact the pixel-defining layer.

[0013] The pixel electrode can include a reflective material, and the opposite electrode can include a transparent material.

[0014] The pixel electrode can include a second transparent conductive oxide layer, a transmissive metal layer, and a first transparent conductive oxide layer that are sequentially stacked on the substrate.

[0015] A protective layer can be further formed on the source electrode and the drain electrode.

[0016] The protective layer can include a transparent conductive oxide.

[0017] The OLED display can further include a pad electrode formed on a same layer as the source electrode and the drain electrode.

[0018] A protective layer including a transparent conductive oxide can be further formed on the pad electrode.

[0019] A thickness of the planarization layer where the planarization layer covers edges of the pad electrode can be less than a thickness of the planarization layer where the planarization layer covers the source electrode and the drain electrode.

[0020] Another aspect is a method of manufacturing an OLED display that includes operations of performing a first mask process for forming an active layer of a thin-film transistor and a first electrode of a capacitor on a substrate; performing a second mask process for forming a gate insulating layer, forming a gate electrode of the thin-film transistor on the gate insulating layer, and forming an etching preventing layer in a region of the gate insulating layer so as to correspond to the first electrode; performing a third mask process for forming an interlayer insulating layer, and forming, in the interlayer insulating layer, a contact hole for exposing a portion of the active layer and a first opening for exposing the etching preventing layer; performing a fourth mask process for forming a source electrode and a drain electrode of the thin-film transistor on the interlayer insulating layer, and removing the etching preventing layer; performing a fifth mask process for forming a planarization layer, forming a contact hole for exposing one of the source electrode and the drain electrode in the planarization layer, and forming a second opening in the first opening; performing a sixth mask process for forming a pixel electrode on the planarization layer, and forming a second electrode of the capacitor in the second opening; and performing a seventh mask process for forming a pixel-defining layer for covering edges of the pixel electrode, and the second electrode.

[0021] After the operation of performing the second mask process, the method can further include an operation of doping a resultant of the second mask process with ion impurities on.

[0022] In the third mask process, the contact hole and the first opening can be formed by dry etching.

[0023] After the operation of performing the fourth mask process, the method can further include an operation of doping a resultant of the fourth mask process with ion impurities.

[0024] In the fourth mask process, a pad electrode can be further formed along with the source electrode and the drain electrode.

[0025] A thickness of the planarization layer where the planarization layer covers edges of the pad electrode can be less than a thickness of the planarization layer where the planarization layer covers the source electrode and the drain electrode.

[0026] After the operation of performing the seventh mask process, the method can further include operations of forming an emission layer on the pixel electrode; and forming an opposite electrode on the emission layer.

[0027] Another aspect is an organic light-emitting diode (OLED) display, comprising: a substrate; a thin-film transistor comprising an active layer, a gate electrode, a source electrode, and a drain electrode formed over the substrate; a

gate insulating layer formed between the active layer and the gate electrode; an interlayer insulating layer formed between the gate electrode and the source and drain electrodes; a planarization layer formed over the source and drain electrodes; a pixel electrode formed over the planarization layer; a capacitor comprising a first electrode formed on the same layer as the active layer and a second electrode formed of the same material as the pixel electrode; a pixel-defining layer covering opposing ends of the pixel electrode; an emission layer formed over the pixel electrode; and an opposite electrode formed over the emission layer.

[0028] In the above OLED display, the first electrode includes an ion impurity-doped semiconductor.

[0029] In the above OLED display, a bottom surface of the second electrode contacts the gate insulating layer.

[0030] In the above OLED display, a first opening is formed in the interlayer insulating layer and formed over the first electrode, wherein a second opening is formed in the first opening and has a bottom surface having a width that is less than a width of a bottom surface of the first opening, and wherein the second electrode is formed in the second opening.

[0031] In the above OLED display, the planarization layer covers side surfaces of the first opening.

[0032] In the above OLED display, a top surface of the second electrode contacts the pixel-defining layer.

[0033] In the above OLED display, the pixel electrode is formed of a reflective material, wherein the opposite electrode is formed of a transparent material.

[0034] In the above OLED display, the pixel electrode comprises a second transparent conductive oxide layer, a reflective metal layer, and a first transparent conductive oxide layer that are sequentially stacked over the substrate.

[0035] The above OLED display further comprises a protective layer is formed over the source and drain electrodes.

[0036] In the above OLED display, the protective layer is formed of a transparent conductive oxide.

[0037] The above OLED display further comprises a pad electrode formed on the same layer as the source and drain electrodes.

[0038] The above OLED display further comprises a protective layer formed of a transparent conductive oxide and formed over the pad electrode.

[0039] In the above OLED display, the thickness of the planarization layer where the planarization layer is formed over opposing sides of the pad electrode is less than the thickness of the planarization layer where the planarization layer is formed over the source and drain electrodes.

[0040] Another aspect is a method of manufacturing an organic light-emitting diode (OLED) display, the method comprising: performing a first mask process including forming an active layer of a thin-film transistor and a first electrode of a capacitor over a substrate; performing a second mask process including forming a gate insulating layer, forming a gate electrode of the thin-film transistor over the gate insulating layer, and forming an etching preventing layer in a region of the gate insulating layer corresponding to the first electrode; performing a third mask process including forming an interlayer insulating layer, forming a contact hole in the interlayer insulating layer so as to expose a portion of the active layer, and forming a first opening in the interlayer insulating layer so as to expose the etching preventing layer; performing a fourth mask process including forming source and drain electrodes of the thin-film transistor over the interlayer insulating layer, and removing the etching preventing layer; performing a fifth mask process including forming a planarization layer, forming a contact hole so as to expose one of the source and drain electrodes in the planarization layer, and forming a second opening in the first opening; performing a sixth mask process including forming a pixel electrode over the planarization layer and forming a second electrode of the capacitor in the second opening; and performing a seventh mask process of forming a pixel-defining layer so as to cover the second electrode and opposing sides of the pixel electrode.

lating layer, and removing the etching preventing layer; performing a fifth mask process including forming a planarization layer, forming a contact hole so as to expose one of the source and drain electrodes in the planarization layer, and forming a second opening in the first opening; performing a sixth mask process including forming a pixel electrode over the planarization layer and forming a second electrode of the capacitor in the second opening; and performing a seventh mask process of forming a pixel-defining layer so as to cover the second electrode and opposing sides of the pixel electrode.

[0041] The above method further comprises doping a resultant of the second mask process with ion impurities following the performing of the second mask process.

[0042] In the above method, in the third mask process, dry etching the interlayer insulating layer so as to form the contact hole and the first opening.

[0043] The above method further comprises doping a resultant of the fourth mask process with ion impurities following the performing of the fourth mask process.

[0044] In the above method, the performing of the fourth mask process further includes forming a pad electrode concurrently with the source and drain electrodes.

[0045] In the above method, the thickness of the planarization layer where the planarization layer is formed over opposing sides of the pad electrode is less than the thickness of the planarization layer where the planarization layer is formed over the source and drain electrodes.

[0046] The above method further comprises: forming an emission layer over the pixel electrode following the performing of the seventh mask process; and forming an opposite electrode over the emission layer.

BRIEF DESCRIPTION OF THE DRAWINGS

[0047] FIG. 1 illustrates a plan view of an OLED display according to an exemplary embodiment.

[0048] FIG. 2 illustrates a cross-sectional view illustrating a portion of an emission pixel and a portion of a pad of the OLED display according to the exemplary embodiment.

[0049] FIG. 3 illustrates a cross-sectional view illustrating a first mask process for the OLED display, according to an exemplary embodiment.

[0050] FIGS. 4A and 4B illustrate cross-sectional views illustrating a second mask process for the OLED display, according to an exemplary embodiment.

[0051] FIG. 5 illustrates a cross-sectional view of a resultant of a third mask process for the OLED display, according to an exemplary embodiment.

[0052] FIGS. 6A and 6B illustrate cross-sectional views illustrating a fourth mask process for the OLED display, according to an exemplary embodiment.

[0053] FIG. 7 illustrates a cross-sectional view illustrating a fifth mask process for the OLED display, according to an exemplary embodiment.

[0054] FIG. 8 illustrates a cross-sectional view illustrating a sixth mask process for the OLED display, according to an exemplary embodiment.

[0055] FIG. 9 illustrates a cross-sectional view illustrating a seventh mask process for the OLED display, according to an exemplary embodiment.

DETAILED DESCRIPTION OF CERTAIN INVENTIVE EMBODIMENTS

[0056] As the described technology allows for various changes and numerous embodiments, particular embodiments will be illustrated in the drawings and described in detail in the written description. Effects and features of the described technology and methods of accomplishing the same can be understood more readily by reference to the following detailed description of exemplary embodiments and the accompanying drawings. The described technology can, however, be embodied in many different forms and should not be construed as being limited to the embodiments set forth herein.

[0057] Hereinafter, one or more exemplary embodiments will be described below in more detail with reference to the accompanying drawings. Those components that are the same or are in correspondence are rendered the same reference numeral regardless of the figure number, and redundant explanations are omitted.

[0058] Hereinafter, in one or more exemplary embodiments, while such terms as “first,” “second,” etc., can be used, but such components must not be limited to the above terms, and the above terms are used only to distinguish one component from another.

[0059] Hereinafter, in one or more exemplary embodiments, a singular form can include plural forms, unless there is a particular description contrary thereto.

[0060] Hereinafter, in one or more exemplary embodiments, terms such as “comprise” or “comprising” are used to specify existence of a recited feature or component, not excluding the existence of one or more other recited features or one or more other components.

[0061] Hereinafter, in one or more exemplary embodiments, it will also be understood that when an element such as layer, region, or component is referred to as being “on” another element, it can be directly on the other element, or intervening elements such as layer, region, or component can also be interposed therebetween.

[0062] In the drawings, for convenience of description, the sizes of layers and regions are exaggerated for clarity. For example, a size and thickness of each element can be random for convenience of description, thus, one or more exemplary embodiments are not limited thereto.

[0063] As used herein, the term “and/or” includes any and all combinations of one or more of the associated listed items. In this disclosure, the term “substantially” includes the meanings of completely, almost completely or to any significant degree under some applications and in accordance with those skilled in the art. The term “connected” can include an electrical connection.

[0064] FIG. 1 illustrates a plan view of an OLED display 1 according to an exemplary embodiment. FIG. 2 illustrates a cross-sectional view illustrating a portion of an emission pixel and a portion of a pad of the OLED display 1 according to the first exemplary embodiment.

[0065] Referring to FIG. 1, the OLED display 1 includes a display area DA on a substrate 10, and the display area DA includes a plurality of pixels P and thus displays an image. The display area DA is formed within a sealing line SL, and an encapsulation member (not shown) is arranged to encapsulate the display area DA along the sealing line SL.

[0066] Referring to FIG. 2, a pixel region PXL1 having at least one emission layer 121, a thin-film transistor region TR1 having at least one thin-film transistor, a capacitor region

CAP1 having at least one capacitor, and a pad region PAD1 are arranged on the substrate 10.

[0067] In the thin-film transistor region TR1, an active layer 212 of the thin-film transistor is arranged above the substrate 10 and a buffer layer 11.

[0068] The substrate 10 can be a transparent substrate including a glass substrate, a plastic substrate including polyethylene terephthalate (PET), polyethylene naphthalate (PEN), polyimide, or the like.

[0069] The buffer layer 11 can be further arranged on the substrate 10 so as to form a planar surface on the substrate 10 and to prevent penetration of foreign substances. The buffer layer 11 can be formed as a single layer or a multilayer formed of silicon nitride and/or silicon oxide.

[0070] The active layer 212 is arranged on the buffer layer 11 in the thin-film transistor region TR1. The active layer 212 can be formed of a semiconductor including amorphous silicon or polysilicon.

[0071] The active layer 212 can include a channel region 212c, and a source region 212b and a drain region 212a that are arranged at both sides of the channel region 212c and are doped with impurity. A material of the active layer 212 is not limited to amorphous silicon or polysilicon and can include an oxide semiconductor.

[0072] A gate insulating layer 13 is arranged on the active layer 212. The gate insulating layer 13 can be formed as a single layer or a multilayer including silicon nitride and/or silicon oxide.

[0073] A gate electrode 214 is arranged on the gate insulating layer 13. The gate electrode 214 can be formed as a single layer or multiple layers formed of at least one metal material selected from aluminum (Al), platinum (Pt), palladium (Pd), silver (Ag), magnesium (Mg), gold (Au), nickel (Ni), neodymium (Nd), iridium (Ir), chrome (Cr), lithium (Li), calcium (Ca), molybdenum (Mo), titanium (Ti), tungsten (W), and copper (Cu).

[0074] Although not illustrated in FIG. 2, a wiring such as a scan line can be formed on the same layer as the gate electrode 214 by using the same material as the gate electrode 214.

[0075] As the size of a screen of the OLED display 1 is increased, a thickness of the wiring usually increases so as to prevent a signal delay due to the large screen. In the present embodiment, a thickness of the gate electrode 214 and the wiring can be set between about 6,000 Å and about 12,000 Å. When the thickness of the gate electrode 214 and the wiring is substantially equal to or greater than about 6,000 Å, the signal delay can be prevented in a large screen of at least about 50 inches. And it is difficult to form, via deposition, the thickness of the gate electrode 214 and the wiring to be greater than about 12,000 Å. The above range can provide an optimum balance between reducing signal delay and reducing difficulty in deposition.

[0076] An interlayer insulating layer 15 is deposited on the gate electrode 214. The interlayer insulating layer 15 can be formed as a single layer or multiple layers formed of silicon nitride and/or silicon oxide.

[0077] A source electrode 216b and a drain electrode 216a are arranged on the interlayer insulating layer 15. Each of the source electrode 216b and the drain electrode 216a can be formed as a single layer or multiple layers formed of at least one metal material selected from aluminum (Al), platinum (Pt), palladium (Pd), silver (Ag), magnesium (Mg), gold (Au), nickel (Ni), neodymium (Nd), iridium (Ir), chrome

(Cr), lithium (Li), calcium (Ca), molybdenum (Mo), titanium (Ti), tungsten (W), copper (Cu), and an alloy thereof.

[0078] A protective layer **418** is formed on the source electrode **216b** and the drain electrode **216a**. The protective layer **418** prevents the source electrode **216b** and the drain electrode **216a** from being exposed to an etchant while a pixel electrode **120** is etched, so that a defect can be prevented.

[0079] Since the protective layer **418** and the source electrode **216b**, and the protective layer **418** and the drain electrode **216a** are etched by using the same mask, etched surfaces of edges of the protective layer **418** and the source electrode **216b** can be equal to each other, and etched surfaces of edges of the protective layer **418** and the drain electrode **216a** can be equal to each other.

[0080] A planarization layer **19** that covers the source electrode **216b** and the drain electrode **216a** is formed on the source electrode **216b** and the drain electrode **216a**. The planarization layer **19** can include polymer derivatives having commercial polymers (PMMA and PS) and a phenol group, an acryl-based polymer, an imide-based polymer, an allyl ether-based polymer, an amide-based polymer, a fluorine-based polymer, a p-xylene-based polymer, a vinyl alcohol-based polymer, or a combination thereof.

[0081] The pixel electrode **120** is arranged on the planarization layer **19**. The pixel electrode **120** contacts one of the source electrode **216b** and the drain electrode **216a** via a contact hole **C6** formed in the planarization layer **19**. Referring to FIG. 2, the pixel electrode **120** contacts the drain electrode **216a**, but embodiments are not limited thereto. That is, the pixel electrode **120** can contact the source electrode **216b**.

[0082] The pixel electrode **120** can be formed of a reflective material. The pixel electrode **120** can include a transfective metal layer **120b**. Also, the pixel electrode **120** can further include a first transparent conductive oxide layer **120a** and a second transparent conductive oxide layer **120c** that are formed below and on the transfective metal layer **120b**, respectively.

[0083] The transfective metal layer **120b** can be formed of Ag or a silver alloy. The transfective metal layer **120b** and an opposite electrode **122** that is a transmissive electrode to be described later can form a micro-cavity structure and thus can improve a luminescent efficiency of the OLED display **1**.

[0084] Each of the first and second transparent conductive oxide layers **120a** and **120c** can be formed of at least one material selected from indium tin oxide (ITO), indium zinc oxide (IZO), zinc oxide (ZnO), indium oxide (In_2O_3), indium gallium oxide (IGO), and aluminum zinc oxide (AZO). The first transparent conductive oxide layer **120a** can reinforce adhesion of the planarization layer **19** and the transfective metal layer **120b**, and the second transparent conductive oxide layer **120c** can function as a barrier layer for protecting the transfective metal layer **120b**.

[0085] A metal material such as silver that is highly reducible and forms the transfective metal layer **120b** can cause a problem by which a silver particle is extracted while the pixel electrode **120** is etched. The extracted silver particle can be a main factor of a particle defect that causes a dark spot. While the pixel electrode **120** including silver is etched, if the source electrode **216b**, the drain electrode **216a**, a pad electrode **416**, or other wiring is exposed to an etchant, silver ion that is highly reducible can receive an electron from the aforementioned metal materials and can be re-extracted as a silver particle. However, in the OLED display **1** according to the

present embodiment, the source electrode **216b**, the drain electrode **216a**, and the pad electrode **416** are protected by the protective layer **418** and thus are not exposed to the etchant. Therefore, the defect due to the re-extraction of the silver particle can be prevented.

[0086] The edges of the pixel electrode **120** are covered by a pixel-defining layer **20**. The pixel-defining layer **20** can be formed of polymer derivatives having commercial polymers (PMMA and PS) and a phenol group, an acryl-based polymer, an imide-based polymer, an allyl ether-based polymer, an amide-based polymer, a fluorine-based polymer, a p-xylene-based polymer, a vinyl alcohol-based polymer, or a combination thereof.

[0087] An intermediate layer (not shown) that includes the emission layer **121** is arranged on the pixel electrode **120** whose top surface is exposed by an opening **C5** formed in the pixel-defining layer **20**. The emission layer **121** can be formed of a small molecule organic material or a polymer organic material.

[0088] If the emission layer **121** is formed of the small molecule organic material, the intermediate layer can further include a hole transport layer (HTL), a hole injection layer (HIL), an electron transport layer (ETL), or an electron injection layer (EIL). In addition to these layers, if required, the intermediate layer can further include various layers. Here, various organic materials including copper phthalocyanine (CuPc), N,N'-Di(naphthalene-1-yl)-N,N-diphenyl-benzidine (NPB), tris-8-hydroxyquinoline aluminum (Alq3), or the like can be used.

[0089] If the emission layer **121** is formed of the polymer organic material, the intermediate layer can further include an HTL. The HTL can be formed of poly-(2,4)-ethylene-dihydroxy thiophene (PEDOT) or polyaniline (PANI). Here, the polymer organic material can include poly-phenylene vinylene (PPV), polyfluorene, or the like. Also, an inorganic material can be further arranged between the emission layer **121** and pixel electrode **120** and can be further arranged between the emission layer **121** and the opposite electrode **122**.

[0090] Referring to FIG. 2, the emission layer **121** is formed in a second opening **C8**, but this is only for convenience of description and one or more exemplary embodiments are not limited thereto. The emission layer **121** can be formed not only in the second opening **C8** but can also extend to a top surface of the pixel-defining layer **20** along an etched surface of the second opening **C8** formed in the pixel-defining layer **20**.

[0091] The opposite electrode **122** that is commonly formed in pixels is arranged on the emission layer **121**. In the OLED display **1** according to the present embodiment, the pixel electrode **120** is used as an anode and the opposite electrode **122** is used as a cathode, but polarities of the electrodes can be switched.

[0092] The opposite electrode **122** can be the transmissive electrode formed of a transparent material. The opposite electrode **122** can be formed of at least one material selected from Al, Mg, Li, Ca, LiF/Ca, and LiF/Al and can have an appropriate thickness sufficient to transmit light. Light that is emitted from the emission layer **121** is reflected from the pixel electrode **120**, passes through the opposite electrode **122** that is the transmissive electrode, and is discharged in a direction away from the substrate **10**.

[0093] In some embodiments, the opposite electrode 122 is not separately formed in each pixel but can be a common electrode that wholly covers the display area DA (refer to FIG. 1).

[0094] A capacitor formed in the capacitor region CAP1 includes a first electrode 312 formed on the same layer as the active layer 212 and a second electrode 320 formed of the same material as the pixel electrode 120. The gate insulating layer 13 formed between the first electrode 312 and the second electrode 320 operates as a dielectric layer.

[0095] The first electrode 312 can be formed of the same material as the active layer 212. In more detail, the first electrode 312 can include a semiconductor that is doped with ion impurities. The ion impurities can be the same as the ion impurities included in the source electrode 216b and the drain electrode 216a of the thin-film transistor.

[0096] The gate insulating layer 13 is formed on the first electrode 312. The second electrode 320 of the capacitor is formed on the gate insulating layer 13 and directly contacts the gate insulating layer 13.

[0097] The gate insulating layer 13 formed between the active layer 212 and the gate electrode 214 of the thin-film transistor extends to the capacitor region CAP1, and thus is also formed between the first electrode 312 and the second electrode 320. Accordingly, the gate insulating layer 13 operates as the dielectric layer of the capacitor.

[0098] The interlayer insulating layer 15 formed between the gate electrode 214 and the source and drain electrodes 216b and 216a of the thin-film transistor is removed from a region on the first electrode 312 in the capacitor region CAP1. A first opening C2 is formed in the region from which the interlayer insulating layer 15 is removed. Accordingly, in the present embodiment, the interlayer insulating layer 15 does not operate as a dielectric layer of the capacitor.

[0099] The planarization layer 19 formed between the source and drain electrodes 216b and 216a of the thin-film transistor and the pixel electrode 120 is removed from a region on the first electrode 312 in the capacitor region CAP1. The second opening C8 is formed in the region from which the planarization layer 19 is removed.

[0100] The second opening C8 is formed inside the first opening C2 and has a width less than a width of the first opening C2. That is, the planarization layer 19 is formed to cover side surfaces of the first opening C2 formed in the interlayer insulating layer 15. Since the planarization layer 19 is removed from the region on the first electrode 312, in the present embodiment, the planarization layer 19 does not operate as a dielectric layer of the capacitor.

[0101] Therefore, in the capacitor of the present embodiment, the first electrode 312 is formed of the same material as the doped active layer 212, the second electrode 320 is formed of the same material as the pixel electrode 120, and only the gate insulating layer 13 is used as the dielectric layer, thus, the capacitance of the capacitor can be increased. If the capacitance of the capacitor is increased, it is possible to satisfy a demand for a capacitor having a large capacitance due to a complicated driving circuit for driving an OLED display.

[0102] The second electrode 320 of the capacitor is formed in the second opening C8 formed in the planarization layer 19. The second electrode 320 is formed of the same material as the pixel electrode 120. As will be described later, the second electrode 320 and the pixel electrode 120 are formed in a same photo mask process.

[0103] The second opening C8 formed from an organic insulating layer is patterned by dry etching, and covers an etched surface of the first opening C2 having a sharp slope and a rough surface, so that the second electrode 320 can be effectively formed in the second opening C8.

[0104] The second electrode 320 includes a first portion 320a formed on a bottom of the second opening C8, and a second portion 320b formed on each of side surfaces of the second opening C8.

[0105] One surface of the first portion 320a directly contacts the gate insulating layer 13, and the other surface of the first portion 320a directly contacts the pixel-defining layer 20. One surface of the second portion 320b directly contacts the planarization layer 19, and the other surface of the first portion 320a directly contacts the pixel-defining layer 20.

[0106] In the pad region PAD1 that is an outer region of the display area DA, the pad electrode 416 that is a connection terminal of an external driver is positioned.

[0107] The pad electrode 416 is formed on the interlayer insulating layer 15, and edges of the pad electrode 416 are covered with the planarization layer 19.

[0108] The pad electrode 416 is formed of the same material as the source electrode 216b and the drain electrode 216a, and the protective layer 418 is formed on the pad electrode 416. The protective layer 418 prevents the pad electrode 416 from being exposed to an etchant while the pixel electrode 120 is etched, so that a particle defect can be prevented. Also, the protective layer 418 prevents the pad electrode 416 from being exposed to moisture and oxygen, so that it is possible to prevent reliability of a pad from deteriorating.

[0109] Since the protective layer 418 and the pad electrode 416 are etched by using the same mask, etched surfaces of edges of the protective layer 418 and the pad electrode 416 can be substantially equal to each other.

[0110] A thickness of the planarization layer 19 where the planarization layer 19 covers the edges of the pad electrode 416 is less than a thickness of the planarization layer 19 where the planarization layer 19 covers the source electrode 216b and the drain electrode 216a in the thin-film transistor region TR1, and is less than a thickness of the planarization layer 19 where the planarization layer 19 is between the interlayer insulating layer 15 and the pixel electrode 120 in the pixel region PXL1.

[0111] The planarization layer 19 covers the edges of the pad electrode 416 and thus prevents deterioration of the edges of the pad electrode 416. However, if the thickness of the planarization layer 19 where the planarization layer 19 covers the edges of the pad electrode 416 is large, a connection error can occur at the pad electrode 416 when the external driver is connected, and thus, the thickness of the planarization layer 19 where the planarization layer 19 covers the edges of the pad electrode 416 can be small.

[0112] Although not illustrated in FIG. 2, the OLED display 1 can further include an encapsulation member (not shown) that encapsulates the pixel region PXL1, the capacitor region CAP1, and the thin-film transistor region TR1. The encapsulation member can be formed as a substrate including a glass material, a metal film, or an encapsulation thin film formed of an organic insulating film and an inorganic insulating film that are alternately stacked.

[0113] Hereinafter, a method of manufacturing the OLED display 1 will be described with reference to FIGS. 3 through 9.

[0114] FIG. 3 illustrates a cross-sectional view illustrating a first mask process for the OLED display 1, according to an exemplary embodiment.

[0115] Referring to FIG. 3, the buffer layer 11 is formed on the substrate 10, and a semiconductor layer (not shown) is formed on the buffer layer 11 and then is patterned so as to form the active layer 212 of the thin-film transistor and the first electrode 312 of the capacitor.

[0116] Although not illustrated, after photoresist (not shown) is coated on the semiconductor layer, the semiconductor layer is patterned via a photolithography process using a first photomask (not shown), so that the active layer 212 is formed. The photolithography process is processed in a manner that the first photomask is exposed by an exposure device (not shown), and then developing, etching, and stripping or ashing processes are sequentially performed.

[0117] The semiconductor layer can be formed of amorphous silicon or poly silicon. Here, the poly silicon can be formed by crystallizing the amorphous silicon. The crystallization of the amorphous silicon can be performed by using various methods including a rapid thermal annealing (RTA) method, a solid phase crystallization (SPC) method, an excimer laser annealing (ELA) method, a metal induced crystallization (MIC) method, a metal induced lateral crystallization (MILC) method, a sequential lateral solidification (SLS) method, and the like. However, a method for the semiconductor layer is not limited to the amorphous silicon or the poly silicon and can include an oxide semiconductor.

[0118] FIGS. 4A and 4B illustrate cross-sectional views illustrating a second mask process for the OLED display 1, according to an exemplary embodiment.

[0119] Referring to FIG. 4A, the gate insulating layer 13 is formed on the resultant of the first mask process shown in FIG. 3, and a first metal layer (not shown) is formed on the gate insulating layer 13 and is patterned. The first metal layer can be formed as a single layer or multiple layers formed of at least one metal material selected from Al, Pt, Pd, Ag, Mg, Au, Ni, Nd, Ir, Cr, Li, Ca, Mo, Ti, W, and Cu.

[0120] As a patterning result, the gate electrode 214 and an etching preventing layer 314 are formed on the gate insulating layer 13. The gate electrode 214 is formed while corresponding to the channel region 212c of the active layer 212, and the etching preventing layer 314 is formed while corresponding to the first electrode 312 of the capacitor.

[0121] Referring to FIG. 4B, ion impurity is first doped on the aforementioned structure. The ion impurity including b-type ion or p-type ion can be doped. Ion impurity with a density of at least about 1×10^{15} atoms/cm² can be doped while targeting the active layer 212 of the thin-film transistor.

[0122] The active layer 212 is doped with the ion impurity by using the gate electrode 214 as a self-align mask, so that the active layer 212 has the source region 212b and the drain region 212a, and the channel region 212c therebetween that are doped with the ion impurity.

[0123] FIG. 5 illustrates a cross-sectional view of a resultant of a third mask process for the OLED display 1, according to an exemplary embodiment.

[0124] The interlayer insulating layer 15 is formed on a resultant of the second mask process shown in FIG. 4B, and is patterned so as to form contact holes C3 and C4 for exposing the source region 212b and the drain region 212a of the active layer 212, and the first opening C2 for exposing the etching preventing layer 314.

[0125] The third mask process of forming the contact holes C3 and C4 and the first opening C2 by patterning the interlayer insulating layer 15 can be performed by dry etching. The etching preventing layer 314 is formed on the first electrode 312 and prevents etching of the gate insulating layer 13 that operates as a dielectric layer in the present embodiment.

[0126] FIGS. 6A and 6B illustrate cross-sectional views illustrating a fourth mask process for the OLED display 1, according to an exemplary embodiment.

[0127] Referring to FIG. 6A, a second metal layer (not shown) and the protective layer 418 are formed on the resultant of the third mask process shown in FIG. 5 and are patterned so as to substantially simultaneously or concurrently form the source electrode 216b and the protective layer 418, the drain electrode 216a and the protective layer 418, and the pad electrode 416 and the protective layer 418.

[0128] Here, while the second metal layer and the protective layer 418 are patterned, the etching preventing layer 314 in the capacitor region CAP1 is removed along with the second metal layer on the etching preventing layer 314.

[0129] The second metal layer can be formed as at least two different metal layers having different electron mobilities. For example, the second metal layer is formed as at least two different metal layers formed of metal materials selected from Al, Pt, Pd, Ag, Mg, Au, Ni, Nd, Ir, Cr, Li, Ca, Mo, Ti, W, Cu, and an alloy thereof.

[0130] The protective layer 418 can be a transparent conductive oxide layer including at least one material selected from the group consisting of ITO, IZO, ZnO, In₂O₃, IGO, and AZO.

[0131] Referring to FIG. 6B, the aforementioned structure is secondly doped with ion impurities of a b-type or a p-type ion. Ion impurity with a density of at least about 1×10^{10} atoms/cm² can be doped while targeting the first electrode 312 of the capacitor. Due to the second doping, capacitance of the capacitor is increased.

[0132] Referring to FIG. 6B, only the first electrode 312 of the capacitor is doped, but in some embodiments, wirings that are formed on the same layer as the first electrode 312 and are connected to the first electrode 312 are also doped, so that an electric conductivity is increased.

[0133] FIG. 7 illustrates a cross-sectional view illustrating a fifth mask process for the OLED display 1, according to an exemplary embodiment.

[0134] Referring to FIG. 7, the planarization layer 19 is formed on the resultant of the fourth mask process shown in FIG. 6B and is patterned, so that the contact hole C6 for exposing a portion of the drain electrode 216a, a contact hole C7 for exposing a top surface of the protective layer 418 on the pad electrode 416, and the second opening C8.

[0135] Referring to FIG. 7, the contact hole C6 is formed in the drain electrode 216a but embodiments are not limited thereto. That is, the contact hole C6 can be formed in the source electrode 216b.

[0136] The second opening C8 exposes a top surface of the gate insulating layer 13 formed on the first electrode 312 of the capacitor, and covers etched side surfaces of the first opening C2 formed in the interlayer insulating layer 15.

[0137] Since the interlayer insulating layer 15 is formed from an inorganic insulating layer and is patterned by dry etching, the etched side surfaces of the first opening C2 has a sharp slope, and an etched bottom surface of the first opening C2 is rough. However, in the present embodiment, since the planarization layer 19 formed from an organic insulating

layer is patterned by wet etching and is formed in the first opening C2, the second opening C8 covers the etched side surfaces of the first opening C2, and thus, allows the sharp slope of the etched side surfaces to be gentle and improves a characteristic of the etched bottom surface.

[0138] The contact hole C7 is formed in the planarization layer 19 so as to expose the top surface of the protective layer 418 on the pad electrode 416. Since the thickness of the planarization layer 19 where the planarization layer 19 covers the edges of the pad electrode 416 is less than the thickness of the planarization layer 19 where the planarization layer 19 covers the source electrode 216b and the drain electrode 216a in the thin-film transistor region TR1, and is less than the thickness of the planarization layer 19 where the planarization layer 19 is between the interlayer insulating layer 15 and the pixel electrode 120 in the pixel region PXL1, it is possible to decrease a connection error that occurs at the pad electrode 416 while the external driver is connected.

[0139] The fifth mask process can be performed by using a half-tone mask (not shown).

[0140] FIG. 8 illustrates a cross-sectional view illustrating a sixth mask process for the OLED display 1, according to an exemplary embodiment.

[0141] Referring to FIG. 8, a layer including a reflective material (not shown) is deposited and patterned on the resultant of the fifth mask process shown in FIG. 7, so that the pixel electrode 120 and the second electrode 320 of the capacitor are formed.

[0142] The pixel electrode 120 can include the first transparent conductive oxide layer 120a, the transfective metal layer 120b, and the second transparent conductive oxide layer 120c. Also, the second electrode 320 of the capacitor can be formed of the same material as the pixel electrode 120.

[0143] The second electrode 320 is formed in the second opening C8 formed in the planarization layer 19. The second electrode 320 includes the first portion 320a formed on the bottom of the second opening C8, and the second portion 320b formed on each of the side surfaces of the second opening C8.

[0144] One surface of the first portion 320a directly contacts the gate insulating layer 13, and one surface of the second portion 320b directly contacts the planarization layer 19.

[0145] Since the capacitor has the thin gate insulating layer 13 formed between the first electrode 312 and the second electrode 320 operates as a dielectric layer, capacitance of the capacitor can be increased.

[0146] FIG. 9 illustrates a cross-sectional view illustrating a seventh mask process for the OLED display 1, according to an exemplary embodiment.

[0147] Referring to FIG. 9, the seventh mask process is performed to form the pixel-defining layer 20 on the resultant of the sixth mask process shown in FIG. 8 and then to form the opening C5 for exposing a top surface of the pixel electrode 120.

[0148] A top surface of the second electrode 320 of the capacitor directly contacts the pixel-defining layer 20.

[0149] The pixel-defining layer 20 can be an organic insulating layer formed of polymer derivatives having commercial polymers (PMMA and PS) and a phenol group, an acryl-based polymer, an imide-based polymer, an allyl ether-based polymer, an amide-based polymer, a fluorine-based polymer, a p-xylene-based polymer, a vinyl alcohol-based polymer, or a combination thereof.

[0150] An intermediate layer (not shown) including the emission layer 121 (refer to FIG. 2) is formed on the resultant of the seventh mask process shown in FIG. 9, and the opposite electrode 122 (refer to FIG. 2) is formed.

[0151] In the OLED display 1 according to exemplary embodiments, the first electrode 312 and the second electrode 320 of the capacitor are formed of the same materials as the doped active layer 212 and the pixel electrode 120, respectively, and only the gate insulating layer 13 is used as the dielectric layer. By doing so, the capacitance of the capacitor can be increased.

[0152] Also, since the pixel electrode 120 includes the transfective metal layer 120b, a luminescent efficiency of the OLED display 1 can be improved due to a micro-cavity structure.

[0153] Also, since the OLED display 1 is manufactured through the seven mask processes, the manufacturing costs can be reduced.

[0154] It should be understood that the exemplary embodiments described herein should be considered in a descriptive sense only and not for purposes of limitation. Descriptions of features or aspects within each exemplary embodiment should typically be considered as available for other similar features or aspects in other exemplary embodiments.

[0155] While the inventive technology has been described with reference to the figures, it will be understood by those of ordinary skill in the art that various changes in form and details can be made therein without departing from the spirit and scope as defined by the following claims.

What is claimed is:

1. An organic light-emitting diode (OLED) display, comprising:

- a substrate;
- a thin-film transistor comprising an active layer, a gate electrode, a source electrode, and a drain electrode formed over the substrate;
- a gate insulating layer formed between the active layer and the gate electrode;
- an interlayer insulating layer formed between the gate electrode and the source and drain electrodes;
- a planarization layer formed over the source and drain electrodes;
- a pixel electrode formed over the planarization layer;
- a capacitor comprising a first electrode formed on the same layer as the active layer and a second electrode formed of the same material as the pixel electrode;
- a pixel-defining layer covering opposing ends of the pixel electrode;
- an emission layer formed over the pixel electrode; and
- an opposite electrode formed over the emission layer.

2. The OLED display of claim 1, wherein the first electrode includes an ion impurity-doped semiconductor.

3. The OLED display of claim 1, wherein a bottom surface of the second electrode contacts the gate insulating layer.

4. The OLED display of claim 1, wherein a first opening is formed in the interlayer insulating layer and formed over the first electrode,

wherein a second opening is formed in the first opening and has a bottom surface having a width that is less than a width of a bottom surface of the first opening, and wherein the second electrode is formed in the second opening.

5. The OLED display of claim 4, wherein the planarization layer covers side surfaces of the first opening.

6. The OLED display of claim 1, wherein a top surface of the second electrode contacts the pixel-defining layer.

7. The OLED display of claim 1, wherein the pixel electrode is formed of a reflective material, and wherein the opposite electrode is formed of a transparent material.

8. The OLED display of claim 7, wherein the pixel electrode comprises a second transparent conductive oxide layer, a transmissive metal layer, and a first transparent conductive oxide layer that are sequentially stacked over the substrate.

9. The OLED display of claim 1, further comprising a protective layer is formed over the source and drain electrodes.

10. The OLED display of claim 9, wherein the protective layer is formed of a transparent conductive oxide.

11. The OLED display of claim 1, further comprising a pad electrode formed on the same layer as the source and drain electrodes.

12. The OLED display of claim 11, further comprising a protective layer formed of a transparent conductive oxide and formed over the pad electrode.

13. The OLED display of claim 11, wherein the thickness of the planarization layer where the planarization layer is formed over opposing sides of the pad electrode is less than the thickness of the planarization layer where the planarization layer is formed over the source and drain electrodes.

14. A method of manufacturing an organic light-emitting diode (OLED) display, the method comprising:

performing a first mask process including forming an active layer of a thin-film transistor and a first electrode of a capacitor over a substrate;

performing a second mask process including forming a gate insulating layer, forming a gate electrode of the thin-film transistor over the gate insulating layer, and forming an etching preventing layer in a region of the gate insulating layer corresponding to the first electrode;

performing a third mask process including forming an interlayer insulating layer, forming a contact hole in the interlayer insulating layer so as to expose a portion of the active layer, and forming a first opening in the interlayer insulating layer so as to expose the etching preventing layer;

performing a fourth mask process including forming source and drain electrodes of the thin-film transistor over the interlayer insulating layer, and removing the etching preventing layer;

performing a fifth mask process including forming a planarization layer, forming a contact hole so as to expose one of the source and drain electrodes in the planarization layer, and forming a second opening in the first opening;

performing a sixth mask process including forming a pixel electrode over the planarization layer and forming a second electrode of the capacitor in the second opening; and

performing a seventh mask process of forming a pixel-defining layer so as to cover the second electrode and opposing sides of the pixel electrode.

15. The method of claim 14, further comprising doping a resultant of the second mask process with ion impurities following the performing of the second mask process.

16. The method of claim 14, wherein, in the third mask process, dry etching the interlayer insulating layer so as to form the contact hole and the first opening.

17. The method of claim 14, further comprising doping a resultant of the fourth mask process with ion impurities following the performing of the fourth mask process.

18. The method of claim 14, wherein the performing of the fourth mask process further includes forming a pad electrode concurrently with the source and drain electrodes.

19. The method of claim 18, wherein the thickness of the planarization layer where the planarization layer is formed over opposing sides of the pad electrode is less than the thickness of the planarization layer where the planarization layer is formed over the source and drain electrodes.

20. The method of claim 14, further comprising:

forming an emission layer over the pixel electrode following the performing of the seventh mask process; and

forming an opposite electrode over the emission layer.

* * * * *

专利名称(译)	有机发光二极管显示器及其制造方法		
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摘要(译)

公开了一种有机发光二极管 (OLED) 显示器和制造OLED显示器的方法。在一个方面, 显示器包括衬底和薄膜晶体管, 薄膜晶体管包括形成在衬底上的有源层, 栅电极, 源电极和漏电极。在有源层和栅电极之间形成栅极绝缘层, 并且在栅电极和源电极和漏电极之间形成层间绝缘层。另外, 在源电极和漏电极上形成平坦化层, 并且在平坦化层上形成像素电极。该显示器还包括电容器, 该电容器包括形成在与有源层相同的层上的第一电极和由与像素电极相同的材料形成的第二电极。像素限定层覆盖像素电极的相对端; 在像素电极上形成发光层。

